

REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed March 15, 2004. Applicant respectfully requests reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 102

Claims 1, 3, 7-9, 11-14, 19-20 and 23 stand rejected as anticipated by U.S. Patent No. 5,619,497 ("Gallagher"). In rejecting Claims 1, 9 and 19, the Examiner states that Gallagher shows "making a routing decision for the first frame based upon the header information (Col. 24, 49-50: an identifier of the output port associated with the located D_ID table entry is read from the table by the control circuit 450."

Applicants submit that Claim 1, as amended, recites "making a routing decision for the first frame based upon the header information stored in the header storage", Claim 7 recites that "the transfer logic is configured to make a routing decision for each of the frames in the receive buffer based on the corresponding header information in the header storage" and Claim 19 recites "transfer logic is configured to receive first header information from the header buffer and to make a routing decision based upon the received header information." Each of these Claims share the common feature that the routing decision is made based on header information that comes from header storage. Because routing decisions are made based on header information that comes from header storage, frames can be routed more quickly than if the routing information is extracted from frame itself. This can allow a frame to be immediately transferred to the appropriate transmit buffer according to the routing decision.

Gallagher, on the other hand, teaches a system in which a routing decision is made based on the header information read from a frame. In the system of Gallagher, the transmit frame manager programs the DMA to read data out of system memory and forward the data, along with a corresponding header, to the frame routing circuit 340. The frame routing circuit 340 maintains a D_ID table 454 that includes the D_ID for each node known to be connected to the switch fabric and an identifier for the corresponding port. See col. 24, lines 28-48. The frame routing circuit receives the processed frame (i.e., header and data) on line 338 and stores the frame in a buffer. See col. 24, lines 26-34. When the control circuit of the frame routing circuit receives a processed frame from the frame handler, it compares the "D_ID

specified in the processed frame" to the D_ID table to determine the corresponding port. See col. 24, lines 49-53. Based on the port specified in the D_ID table, the control circuit can position the switch accordingly for the frame. See col. 24, lines 53-55.

Thus, Gallagher teaches that the processed frames (i.e., header and data) are received on a common line and are stored in a buffer of the frame routing circuit. Routing decisions are made based on the "D_ID specified in the processed frame." There is no teaching or suggestion that the header data of the processed frame should be stored in a separate header storage for purposes of making routing decisions. Moreover, the D_ID table is not a header storage because it is simply a predefined lookup table of D_IDS and ports. Applicants, therefore, can not find a teaching or suggestion in the portions of Gallagher cited by the Examiner that the routing decision should be made based on header information from header storage. If the Examiner disagrees, Applicants respectfully request that the Examiner particularly point out where basing a routing decision on header information from header storage can be found in the cited references. Otherwise, Applicants respectfully request withdrawal of the rejections of Claims 1, 9 and 19.

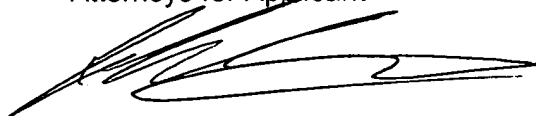
Claims 2-8, 10-18 and 20-23 variously depend from claims 1, 9 and 19. For the reasons discussed above in connection with the §102 rejection, Gallagher neither teaches nor suggests that the routing decision should be made based on header information from header storage. Applicant respectfully requests that the Examiner point out where each of the claimed features can be found in the cited reference or withdraw the rejections of Claims 2-8, 10-18 and 20-23 as further limitations on Claims 1, 9 and 19.

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-0456 of Gray Cary Ware & Freidenrich, LLP.

Respectfully submitted,

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